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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/776,024	02/10/2004	Andrea Pagni	851763.447	9064		
38106 75	590 10/19/2006		EXAM	EXAMINER		
	LECTUAL PROPERTY	COLEMA	COLEMAN, ERIC			
701 FIFTH AV SEATTLE, W	ENUE, SUITE 5400 A 98104-7092	ART UNIT	PAPER NUMBER			
obiriibb, w			2183			
			DATE MAILED: 10/19/2000	6		

Please find below and/or attached an Office communication concerning this application or proceeding.

	·	Applica	tion No.	Applicant(s)					
Office Action Summary		10/776,	024	PAGNI ET AL.					
		Examin	er	Art Unit					
	•	Eric Col	eman	2183					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
A SHORTENED WHICHEVER IS - Extensions of time in after SIX (6) MONTH If NO period for reply - Failure to reply within Any reply received b	STATUTORY PERIOD FO LONGER, FROM THE MA ay be available under the provisions of S from the mailing date of this commu- is specified above, the maximum state the set or extended period for reply of the Office later than three months aff djustment. See 37 CFR 1.704(b).	AILING DATE OF of 37 CFR 1.136(a). In no unication. utory period will apply and will, by statute, cause the a	THIS COMMUNIC event, however, may a will expire SIX (6) MON pplication to become AB	CATION. reply be timely filed NTHS from the mailing date of this of BANDONED (35 U.S.C. § 133).					
Status				•					
2a)☐ This action 3)☐ Since this	e to communication(s) filed is FINAL . 2 application is in condition factordance with the practic	b)⊠ This action is or allowance exce∣	ot for formal mate	•	e merits is				
Disposition of Claims									
4a) Of the 5) ⊠ Claim(s) <u>1</u> 6) ⊠ Claim(s) <u>2</u> 7) ⊠ Claim(s) <u>2</u>	-31 is/are pending in the apabove claim(s) is/are allowed19, 24-31 is/are allowed. 0 and 21 is/are rejected. 2 and 23 is/are objected to are subject to restrict	e withdrawn from o							
Application Papers									
10)∭ The drawin Applicant m Replaceme	cation is objected to by the g(s) filed on is/are: ay not request that any object drawing sheet(s) including redeclaration is objected to	a) accepted or tion to the drawing(s) be held in abeyar uired if the drawing	nce. See 37 CFR 1.85(a). g(s) is objected to. See 37 C	7 7				
Priority under 35 U	.S.C. § 119			•					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 									
· ==	son's Patent Drawing Review (P	ro-948)	Paper No(Summary (PTO-413) (s)/Mail Date Informal Patent Application					
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application 6) Other:									

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 2. Claim 20 is rejected under 35 U.S.C. 102(a) as being anticipated by Yoshida (patent publication No. 2002/0138712 A1).
- 3. Yoshida taught the invention as claimed including a data processing ("DP") system comprising:
- 4. A translator device (as per claim 20) (e.g., see figs. 1,2,3) for translating instructions belonging to a first instruction set that are pipelined scalar processor instructions into instructions belonging to a second instruction set (e.g., see page 4, paragraphs 0050-0051) that are VLIW processor instructions for execution on a VLIW processor (e.g., see pages 2-3, paragraphs 0035-000036) that includes a core (e.g. see page 5, paragraphs 0054 and 0057), the translation subsystem device comprising a translation subsystem designed to receive at input instruction of the first instruction set and supply at output a translation including one or more instructions of the second instruction set(e.g., see page 4, paragraphs 0051-0052); and a translation memory(553) coupled to the translation subsystem and structured to store the translation(e.g., see page 4, paragraph 0051); and a control device (532)for taking the translation from the translation memory and supplying it to the core of the VLIW processor (e.g., see figs. 6

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and 7)[the output on lines 546 and 545 of the control portion is transmitted to output buffer in figure 7 to control output of the buffer].

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (patent publication No. 2002/0138712 A1).

Yoshida taught the invention substantially as claimed including a data processing ("DP") system comprising:

7. A translator device(as per claim 20) (e.g., see figs. 1,2,3) for translating instructions belonging to a first instruction set that are pipelined scalar processor instructions into instructions belonging to a second instruction set (e.g., see page 4, paragraphs 0050-0051) that are VLIW processor instructions for execution on a VLIW processor (e.g., see pages 2-3, paragraphs 0035-000036) that includes a core (e.g. see page 5, paragraphs 0054 and 0057), the translation subsystem device comprising a translation subsystem designed to receive at input instruction of the first instruction set and supply at output a translation including one or more instructions of the second instruction set(e.g., see page 4, paragraphs 0051-0052); and a translation memory(553) coupled to the translation subsystem and structured to store the translation(e.g., see page 4, paragraph 0051); and a control device (532)for taking the

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translation from the translation memory and supplying it to the core of the VLIW processor (e.g, see figs. 6 and 7)[the output on lines 546 and 545 of the control portion is transmitted to output buffer in figure 7 to control output of the buffer].

8. As per claim 21, Yoshida did not expressly detail a code table. Yoshida taught the translation subsystem with a translation memory that was used in the translation and operates based on a manner that would have clearly been facilitated by conventional table access of data for determine a output for corresponding input and which would have been within the level of skill of one of ordinary skill in the art. (e.g., see fig. 15 and page 7, paragraphs 0073-0076). Yoshida however did not expressly detail that the memory that stored the output translation stored a code table. However one of ordinary skill would have been motivated to use the same memory to buffer the output and store the code memory at least to reduce the size of the circuit by reducing the number of memories.

Allowable Subject Matter

- 9. Claims 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 10. Claims 1-19 and 24-31 are allowed.

Response to Arguments

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Applicant's arguments with respect to claims 20-21 have been considered but are most in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN PRIMARY EXAMINER